

Serial No. 09/689,533

Remarks

Claims 1-21, 23-25 and 27-37 are pending in the application. Claim 36 has been amended and claim 37 has been canceled herein. Favorable reconsideration of the application, as amended, is respectfully requested.

I. REJECTION OF CLAIMS 1-21, 23-25 AND 27-37 UNDER 35 USC §103

a. 1-6, 8-21, 23-25 and 27-37

Claims 1-6, 8-21, 23-25 and 27-37 stand rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,963,970 to *Davis* in view of U.S. Patent No. 6,249,838 to *Kon*. Withdrawal of the rejection is respectfully requested for at least the following reasons.

Independent claims 1, 12 and 29 recite an information update count method or apparatus, wherein a predetermined permitted update count is stored in non-volatile memory *in a sector which includes a first program to be executed after a reset*. Claim 21 recites a content usage count managing method, wherein a contents usage count storage area of a non-volatile memory *is in a sector which includes a first program to be executed after a reset*. Claim 25 recites a contents usage count storage apparatus having a contents usage count storage area that includes at least one WORD *in a first sector* of the non-volatile memory, wherein *the first sector* of the non-volatile memory *includes a first program to be executed by the micro processor unit after a reset*.

The above features are advantageous, for example, in that if one attempts to overwrite the predetermined update count or usage count, the first program to be executed after a reset also is overwritten. By overwriting the first program to be executed after a reset, the microprocessor is not properly initialized, which can render the system inoperable. (See, e.g., pg. 14, Ins. 11-30 of the application). Accordingly, the present invention deters one from attempting to erase or "hack" the predetermined update count or usage count.

In the present Office Action, the Examiner admits that *Davis* does not teach or suggest that the predetermined permitted update count is stored in the non-volatile memory *in a sector which includes a first program to be executed after a reset*. However, the Examiner contends that *Kon* teaches this feature, and it would have been

Serial No. 09/689,533

obvious to combine *Davis* and *Kon*, thereby rendering the invention obvious. Applicants respectfully disagree with the Examiner.

The Examiner states that *Kon* teaches a data storage unit that includes a counter initialized to be a number of maximum permissible flash memory erasures, wherein the counter is stored in a header portion of the flash memory. The Examiner also states that the header portion, a sector in the flash memory, includes a boot up program, which is a first program to be executed after a reset. In support, the Examiner cites to column 6, line 36 through column 7, line 35 and column 9, line 44 through column 10, line 28 of *Kon*.

Kon discloses that a number of tests against the counter value can be performed during boot up, and preferably the tests are performed by *logic circuitry positioned on the flash memory*. However, and contrary to the Examiner's contention, the cited portion of *Kon* does not teach or suggest a "*header portion, a sector of the flash memory, includes a boot-up program*". (See pg. 4 of the Office Action).

Apparently, the Examiner is equating the logic circuitry positioned on the flash memory as being in the same sector as the counter. It is respectfully submitted that *Kon* merely discloses that the logic is positioned on the flash memory, without teaching that the logic is stored in the same sector as the counter.

Alternatively (and although not clear), the Examiner may be equating the execution of a boot up program that operates on or otherwise utilizes information stored in the header counter as reading on the above claimed features. Again, it is respectfully submitted that *Kon* has not been shown to teach or suggest that the boot up program is in the same sector as the counter. The fact that a boot up program is executed and operates on the counter data does not teach or suggest that the boot up program is stored in the same sector as the counter data.

The above-cited portion of *Kon* does not teach or suggest that a predetermined update count is stored in the non-volatile memory in a sector which includes a first program to be executed after a reset, as recited in independent claims 1, 12 and 29, or a count storage area of a non-volatile memory is in a sector which includes a first program to be executed after a reset, as recited in claim 21. Further, the cited portion of *Kon* does not teach or suggest a contents usage count storage area that includes at least one WORD in a first sector of the non-volatile memory, wherein the first sector of

Serial No. 09/689,533

the non-volatile memory includes a first program to be executed by the micro processor unit after a reset, as recited in claim 25

Accordingly, withdrawal of the rejection of claims 1, 12, 21, 25 and 29 is respectfully requested.

Claims 2-6, 8-11, 13-20, 23-24, 27-28 and 30-35 depend from one of the independent claim and, therefore, can be distinguished from the cited art for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 2-6, 8-11, 13-20, 23-24, 27-28 and 30-35 is respectfully requested.

b. Claims 36 and 37

Claims 36 and 37 also stand rejected under 35 USC §103(a) based on *Davis and Kon.* Claim 37 has been canceled and thus the rejection of claim 37 is moot. Withdrawal of the rejection of claim 36 is respectfully requested for at least the following reasons.

Claim 36 has been amended and now recites an information update count managing method that includes a step of storing, in a storage area of the non-volatile memory, indicative of a predetermined characteristic, wherein the step of storing comprises initializing a plurality of bits in the information storage area such that the plurality of bits are assigned to be "1", and releasing different ones of the plurality of bits to be "0" each time one of the pieces of information is written in the information storage area *such that a location of the of "0" bits in the information storage area identifies the predetermined characteristic, wherein a total number of "0" bits within the WORD written to the Information storage area does not exceed a predetermined number.*

As disclosed in the application, the apparatus can be configured for operation in specific regions (e.g., the predetermined characteristic). For example, in the regional information, one bit corresponding to the region where the apparatus can be used may be written to a "0" while setting the other bits to "1". In such a case, only one bit of data is supposed to be "0", and the data is considered invalid if two or more bits are "0". Thus, data that has two "0" bits in the regional information is considered invalid. (See, e.g., pg. 15, lines 5-13).

Serial No. 09/689,533

Davis discloses a wear-bar counter that stores erase count information. The data stored in this counter can be any value from 0 to a predetermined maximum value. No mention is found in *Davis* regarding the number of "0" bits in the wear-bar counter. *Davis* has not been found to teach or suggest that the total number of "0" bits within the word written to the information storage area does not exceed a predetermined value, as recited in claim 36. *Kon* and *Sawabe* (U.S. 6,122,434 - discussed below) have not been found to make up for the deficiencies of *Davis*.

Accordingly, withdrawal of the rejection of claim 36 is respectfully requested.

c. Claim 7

Claim 7 stands rejected under 35 USC §103(a) as being unpatentable over *Davis* and *Kon* in view of U.S. Patent No. 6,122,434 to *Sawabe*. Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 7 depends from claim 1 and, as was discussed above, *Davis* and *Kon* have not been found to teach or suggest all the features of claim 1. *Sawabe* is cited for the aspect of teaching an information recording medium that includes regional information. *Sawabe*, however, has not been found to make up for the deficiencies of *Davis* and *Kon*. Accordingly, claim 1 is patentable over *Davis*, *Kon* and *Sawabe*.

Since claim 7 depends from claim 1, it can be distinguished from the cited art for at least the same reasons.

Accordingly, withdrawal of the rejection of claim 7 is respectfully requested.

II. CONCLUSION

Accordingly, claims 1-21, 23-25 and 27-36 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

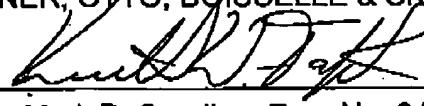
Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Serial No. 09/689,533

In the event any fee or additional fee is due in connection with the filing of this paper, the Commissioner is authorized to charge those fees to our Deposit Account No. 18-0988 (under the above Docket Number).

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

By 

Mark D. Saralino, Reg. No. 34,243

Kenneth W. Fafrak, Reg. No. 50,689

1621 Euclid Avenue
Nineteenth Floor
Cleveland, Ohio 44115
PH: (216) 621-1113
FAX: (216)621-6165
B:\YAMA\P741US\P0741US\Reply_to_OA 6-3-05.wpd

Page 14 of 14

PAGE 14/14 * RCVD AT 8/31/2005 10:06:48 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/26 * DNIS:2738300 * CSID:216 621 6165 * DURATION (mm:ss):04:12

BEST AVAILABLE COPY